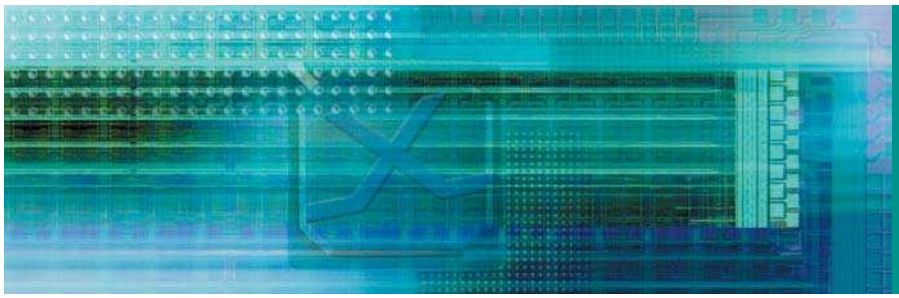


FPGA Family Product Brief

µWatt FPGAs: Ultra-Low Power Programmable Logic Solutions

QuickLogic provides µWatt FPGAs, ultra-low power programmable logic solutions targeted for power-sensitive applications. When your design absolutely needs to meet a tight power budget, QuickLogic devices provide the necessary performance and density while achieving much lower power than alternative solutions.

Applications:

- Handheld Devices
- Portable Medical Equipment
- Portable Industrial/Test Equipment
- Video Imaging/Frame Grabbers
- Data Acquisition/Measurement
- Factory Automation
- Military Systems
- Telecommunications
- Networking

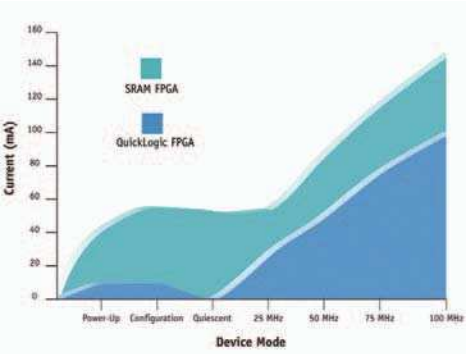
Features:

- Ultra-Low Power Consumption
- Full Featured FPGA Architecture
- High Performance Embedded FIFO Controllers
- Bulletproof Design Security
- Single Chip Small Form Factor Packaging

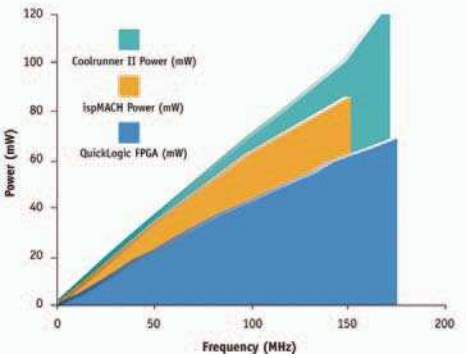
As the complexity of electronic systems grows, the resultant increase in power consumption forces designers to find new ways to control power while still achieving the necessary performance. Handheld and battery-powered device manufacturers continually face this challenge as they try to extend battery life for their customers. In AC-powered systems, this means designers face increased costs of fans and cooling systems, as well as worrying about decreasing system reliability.

QuickLogic eliminates these problems by providing designers with full-featured FPGAs with the industry's lowest power consumption. By employing its patented ViaLink® programmable metal technology, QuickLogic devices achieve ultra-low dynamic power consumption and establish a new baseline in the FPGA industry with standby currents as low as 10 µA. All QuickLogic devices are non-volatile and delivered in small form factor packaging, enabling designers to use FPGAs in even the most space constrained portable electronics systems. Coupling all of these device features with an industry standard FPGA development flow allows our customers to solve their design challenges and shorten their time to market.

QuickLogic FPGAs versus SRAM FPGAs



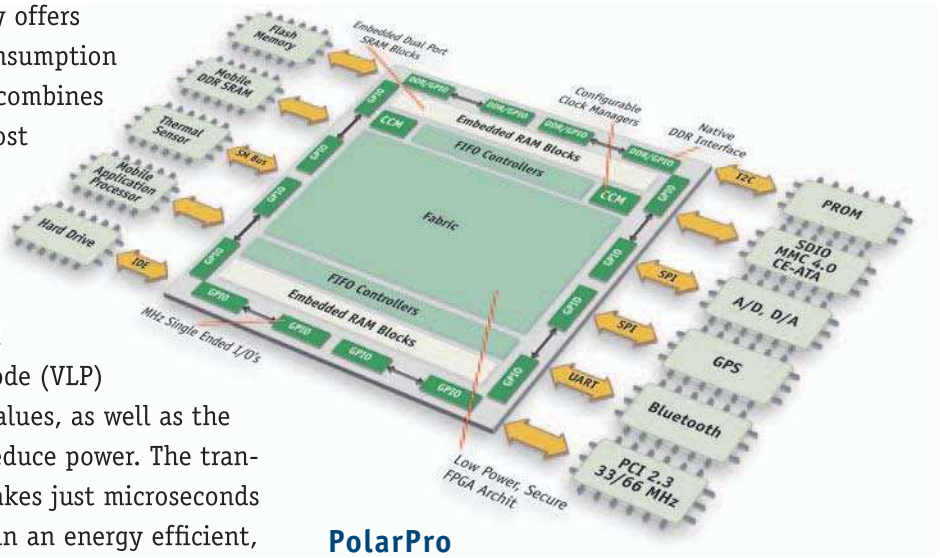
QuickLogic FPGAs versus CPLDs



QUICKLOGIC®

PolarPro™: The Lowest Power FPGA in the Industry

The PolarPro™ family offers the lowest power consumption in the industry and combines it with an expanded feature set that provides a cost effective, small form factor solution for designers in the portable electronics segment. PolarPro has a new, innovative logic cell architecture, versatile embedded memory with built-in FIFO control logic, and an advanced clock management control unit. QuickLogic's new Very Low Power mode (VLP) enables the retention of I/O states and register values, as well as the isolation of the logic array and I/Os in order to reduce power. The transition between VLP mode and normal operation takes just microseconds and draws less than 10 µA. These features result in an energy efficient, cost effective and flexible solution, all offered on a single chip.



PolarPro Block Diagram

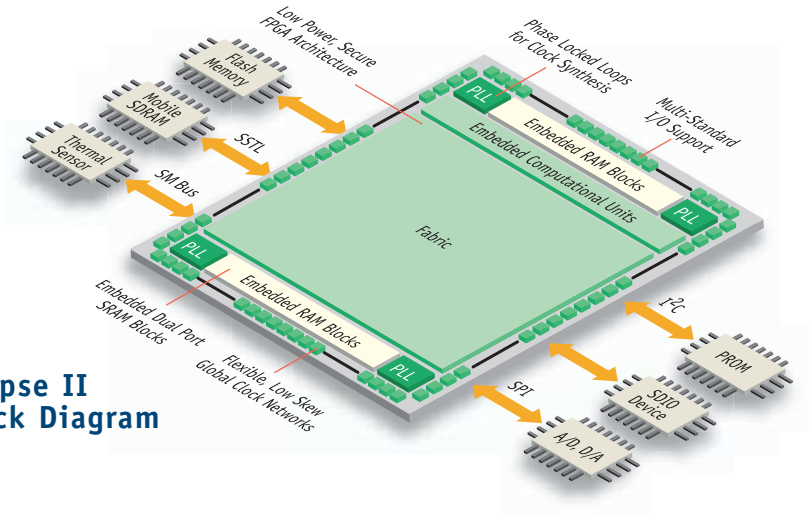
Features	Description and Benefits
Enhanced Logic Cell Architecture	Enables efficient mapping of up to 13-bit wide input functions, 4-input LUT, or two 3-input LUT combinations. Logic cells have four simultaneous outputs and a dedicated Enable D-Type Flip Flop.
VLP Mode	Draws <10 µA, I/O states and internal register values are retained, saves power when function not needed.
Flexible Clock Networks	There are 5 clocks in each of the 4 quadrants. This allows for clocking on one or more quadrants, or on a global clock basis, resulting in a more efficient use of resources.
Programmable I/Os	Each I/O has programmable Slew Rate control, Pull-up/Pull-down and Weak Keeper functionality, supports SSTL3, SSTL2, SSTL18, LVTTL, LVCMOS up to 200MHz and PCI 2.3 up to 66MHz.
CCM–Configurable Clock Manager	Provides clock multiplication and division by 1x, 2x, 4x, and phase shifted clocks by 90, 180 and 270 degrees, with the ability to synchronize internal to external clocks. Provides a programmable delay line that enables clock delays of up to 2.5 ns in steps of 250 ps.
Native Support for DDR SDRAM	Enables system design to leverage lowest cost mobile DDR, DDR1 and DDR2 SDRAM memory.
Embedded SRAM Blocks	Each block is 4,608 bits, with configurable aspect ratios to simplify FIFO design and implementation.
Dedicated FIFO Controller Logic	Requires no logic overhead, enables fast, guaranteed performance, and cost effective FIFO implementations.
Small Form Factor Packaging	Available in small form factor packaging technology, ideal for space constrained applications.

PolarPro Product Table

Device	System Gates	Logic Cells	Max. I/Os	RAM Modules	FIFO Controllers	Dist. Clocks	RAM Bits	CCMs	Packages		
									TFBGA 0.5 mm	TQFP	LBGA 1.0 mm
QL1P075	75,000	512	172	8	8	5	36,864	2	196	144	256
QL1P100	100,000	640	188	8	8	5	36,864	2	196	144	256
QL1P200	200,000	1,536	292	12	12	5	55,296	2	–	–	256/324
QL1P300	300,000	1,920	302	12	12	5	55,296	2	–	–	256/324
QL1P600	600,000	4,224	504	22	22	5	202,752	2	–	–	256/324
QL1P1000	1,000,000	7,680	652	22	22	5	202,752	2	–	–	256/324

Eclipse™ II: Ultra-Low Power FPGAs

The Eclipse II family of low power FPGAs combines the enhanced features of next-generation FPGA devices with power consumption lower than that of CPLDs, giving designers the best of both worlds. Eclipse II has an efficient logic architecture, embedded SRAM blocks for implementing FIFO, RAM or ROM functions and flexible clock networks. All these features result in a cost effective FPGA tailored specifically for portable and handheld electronics applications.



Eclipse II Block Diagram

Features	Description and Benefits
Low Power Consumption	With standby currents as low as 14 µA, the inherent low power consumption reduces system costs through the use of smaller, less costly voltage regulators and power sources.
Bulletproof Design Security	Protects intellectual property from design theft and reverse engineering.
High Performance	315 MHz 16-bit counter performance and 220 MHz 32-bit synchronous FIFO performance.
Single Chip Solution	Provides instant-on capability, eliminating the need for external configuration memory.
Embedded SRAM Blocks	Up to 55 Kbits of embedded Dual-Port SRAM enables integration of FIFO, RAM and ROM functions on chip.
Low Skew Clock Networks	One dedicated clock network hardwired to all clock inputs. Multiple programmable global clock networks allow bridging to as many as 20 clock domains.
User-programmable Phase Locked Loops (PLLs)	User-programmable PLLs can be programmed for clock frequency multiplication and division and can be used to improve I/O timing.
Small Form Factor Packaging	With packaging as small as 8 mm x 8 mm, Eclipse II meets the needs of board-space constrained and portable specifications such as PCMCIA, Cardbus, Mini PCI, and SDIO.

Eclipse II Product Table

Device	System Gates	Logic Cells	Max. Flip-Flops	Max. I/Os	RAM Modules	Dist. Clocks	RAM Bits	Packages						
								VQFP	TFBGA 8x8	TFBGA 12x12	TQFP	PQFP	LFBGA	BGA
QL8025	47,052	128	532	92	4	5	9,216	100	–	196	144	–	–	–
QL8050	63,840	256	884	124	4	5	9,216	100	–	196	144	–	–	–
QL8150	188,946	640	1,709	165	16	5	36,864	–	196	196	144	208	280	–
QL8250	248,160	960	2,670	250	20	9	46,100	–	–	–	–	208	280	484
QL8325	320,640	1,536	4,002	310	24	9	55,300	–	–	–	–	208	280	484

Eclipse/Eclipse Plus FPGAs: High Performance FPGAs

- 600 MHz register-to-register speeds, 225 MHz chip-to-chip speeds
- Clock-to-out delays of less than 3.0 ns
- 248,000 to 662,000 system gates; 275 to 372 I/Os
- 46 KB to 83 KB embedded RAM; up to 300 MHz
- 9 distributed global clocks and 20 quadrant-based local clocks
- JTAG (Joint Test Action Group) support

The Eclipse family of FPGAs offers a host of system-level features for telecommunications, networking, computing, and test applications that require a combination of high performance, high density, and embedded RAM. The Eclipse Plus family of FPGAs combines high-speed dynamically configurable embedded computational units (ECUs), memory, and large amounts of programmable logic. ECUs combine an 8x8-bit multiplier, 16-bit adder, and registers to enable arithmetic and accumulation logic functions.

Eclipse/Eclipse Plus* Product Table

Device	System Gates	Logic Cells	Max. Flip-Flops	Max. I/Os	RAM Modules	Supply Voltage	RAM Bits	ECU	Packages			
									PQFP	FPBGA 0.8 mm	FBGA 1.00 mm	PBGA 1.27 mm
QL6250	248,160	960	2,670	250	20	2.5 V	46,100	–	208	280	484	–
QL7100*	292,160	960	2,670	250	20	2.5 V	46,100	10	208	280	484	–
QL6325	320,640	1,536	3,692	310	24	2.5 V	55,300	–	208	280	484	–
QL7120*	373,440	1,536	3,692	310	24	2.5 V	55,300	12	208	280	484	–
QL6500	488,064	3,072	7,185	372	32	2.5 V	73,700	–	–	280	484	516
QL7160*	558,464	3,072	7,185	372	32	2.5 V	73,700	16	–	280	484	516
QL6600	583,008	4,032	9,105	372	36	2.5 V	82,900	–	–	280	484	516
QL7180*	662,208	4,032	9,105	372	36	2.5 V	82,900	18	–	280	484	516

QuickRAM® FPGAs: 5V Tolerant, High Performance FPGAs

- PCI compliant, 5V I/O tolerant
- Up to 25 KB; Dual-Port Embedded RAM
- 160 MHz FIFOsplus RAM and ROM functions
- 176,000 system gates; 316 I/Os
- JTAG support

The QuickRAM family of FPGAs offers embedded RAM for designs with 5V tolerant I/O, high performance RAM, ROM, and FIFO functions. QuickRAM devices embed up to 25,344 bits of SRAM in an array of configurable logic.

QuickRAM Product Table

Device	System Gates	Logic Cells	Max. Flip-Flops	Max. I/Os	RAM Modules	Supply Voltage	RAM Bits	Packages					
								PLCC	TQFP	PQFP	PBGA	CQFP	CPGA
QL4009	44,964	160	242	82	8	3.3 V	9,216	68/84	100	–	–	–	–
QL4016	61,820	320	438	118	10	3.3 V	11,520	84	100/144	–	–	100	84
QL4036	97,128	672	876	204	14	3.3 V	16,128	–	144	208	256	–	–
QL4058	131,328	1,008	1,260	252	18	3.3 V	20,736	–	–	208/240	456	–	–
QL4090	176,608	1,584	1,900	316	22	3.3 V	25,344	–	–	208/240	456	208	–

pASIC® 3 FPGAs: 5V Tolerant FPGAs

- Up to 400 MHz registered performance
- Up to 75,000 system gates; 82 to 316 I/Os
- Complete, high-performance 3.3 V solutions
- JTAG support
- PCI compliant, 5 V I/O tolerant

pASIC 3 devices deliver high performance 5V tolerant programmable logic. Operating speeds of 400 MHz, pASIC 3 devices have a logic capacity of up to 75,000 gates. Architecture for these devices enables 100 percent routability with fixed pinouts, and provides very high system security and reliability.

pASIC 3 Product Table

Device	System Gates	Logic Cells	Max. Flip-Flops	Max. I/Os	RAM Modules	Supply Voltage	RAM Bits	Packages					
								PLCC	TQFP	PQFP	PBGA	CQFP	CPGA
QL3004	5,188	96	178	82	N/A	3.3 V	N/A	68/84	100	–	–	–	–
QL3004E	5,188	96	178	82	N/A	3.3 V	N/A	68/84	100	–	–	–	–
QL3006	8,003	160	242	82	N/A	3.3 V	N/A	68/84	100	–	–	–	–
QL3012	15,740	320	438	118	N/A	3.3 V	N/A	84	100/144	–	256	–	–
QL3025	32,616	672	876	204	N/A	3.3 V	N/A	–	144	208	256	–	–
QL3040	48,384	1,008	1,260	252	N/A	3.3 V	N/A	–	–	208	456	–	–
QL3060	75,232	1,584	1,900	316	N/A	3.3 V	N/A	–	–	208	456	–	–

Military Temperature FPGAs: Plastic and Ceramic Packaging

- Mil-temp plastic packages up to 125°C
- Mil-temp ceramic and MIL-STD-883C for QuickRAM
- Offers the highest level of design security
- Non-volatile, immune to power fluctuations
- Low power consumption

Electronic content of aerospace systems is growing and FPGAs are playing an increasingly important role. Systems designers are faced with unique challenges including performance over the extended temperature range of –55C to 125C, Single Event Upsets (SEU) and the need for long product life cycles. QuickLogic's Military Temperature FPGAs solve these challenges using ViaLink antifuse technology, offering significant advantages over SRAM FPGAs such as bulletproof design security, instant-on non-volatile logic and the industry's lowest power consumption. In addition, for high altitude applications, QuickLogic has partnered with Aeroflex Corporation to produce radiation hardened FPGAs based on QuickLogic's Eclipse FPGA architecture.

Military Device Product Table

Devices	PolarPro						Eclipse II					Eclipse/Eclipse Plus				QuickPCI				QuickRAM			pASIC 3			
Packages	QL 1P075	QL 1P100	QL 1P200	QL 1P300	QL 1P600	QL 1P1000	QL 8025	QL 8050	QL 8150	QL 8250	QL 8325	QL 6250 7100	QL 6325 7120	QL 6500 7160	QL 6600 7180	QL 5232	QL 5632	QL 5732	QL 5064	QL 4016	QL 4036	QL 4090	QL 3012	QL 3025	QL 3040	QL 3060
84-PLCC																				•			•			
100-VQFP							•	•																		
144-TQFP	•	•					•	•	•																	
196-TFBGA	•	•					•	•	•																	
208-PQFP									•	•	•	•	•			•	•	•			•	•		•	•	•
240-PQFP																						•				
280-FBGA										•	•	•	•	•	•		•	•								
256-PBGA	•	•	•	•	•	•																				
324-PBGA			•	•	•	•																				
456-PBGA																•			•			•				
484-PBGA										•	•	•	•	•	•		•	•	•							
516-PBGA														•	•											
84-CQFP																				•						
100-CQFP																				•						
208-CPGA																•						•				

About QuickLogic

QuickLogic Corporation (NASDAQ: QUIK) is the leading provider of the lowest power programmable logic solutions for the portable electronics, industrial, communications and military markets. Our latest products, PolarPro™, Eclipse™ II and QuickPCI®, are being used to implement bridge and control solutions in embedded systems requiring Wi-Fi and IDE-based hard disk drives.

QuickLogic's proprietary ViaLink® technology offers significant benefits, for programmable logic, including the lowest power, instant-on capability and bulletproof intellectual property security. The company is located at 1277 Orleans Drive, Sunnyvale, CA 94089-1138. Web site www.quicklogic.com

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